1. A digital signal processor capable of performing a Viterbi algorithm comprising:

an instruction fetching unit that fetches instructions;

a decoding unit that decodes the instructions fetched by the instruction fetching unit; and

an execution unit that executes the instructions decoded by the decoding unit, the execution unit comprising:

an arithmetic logic unit configured to perform a register-register arithmetic logic operation,

wherein the arithmetic logic unit compares a first data with a second data, in parallel with a comparison of a third data with a fourth data, and the execution unit outputs new path metrics; and

wherein the first data, the second data, the third data, and the fourth data can each be one of four results obtained by adding one of two path metrics to one of two branch metrics.

2. The digital signal processor according to claim 1, wherein the execution unit outputs any two new path metrics in a high part and a low part of data outputted by the execution unit respectively.

3. The digital signal processor according to claim 2, wherein the execution unit compares the first data with the second data and compares the third data with the fourth data, and outputs new path metrics by one instruction.

4. A digital signal processor capable of performing a Viterbi algorithm comprising:

an instruction fetching unit that fetches instructions;

a decoding unit that decodes the instructions fetched by the instruction fetching unit; and

an execution unit that executes the instructions decoded by the decoding unit, the execution unit comprising:

an arithmetic logic unit configured to perform a register-register arithmetic logic operation;

wherein the arithmetic logic unit compares a first data with a second data, in a single cycle that also includes a comparison of a third data with a fourth data, and the execution unit outputs new path metrics, and

wherein the first data, the second data, the third data, and the fourth data can each be one of four results obtained by adding one of two path metrics to one of two branch metrics.

5. The digital signal processor according to claim 4, wherein the execution unit outputs any

two new path metrics in a high part and a low part of data outputted by the execution unit respectively.

6. The digital signal processor according to claim 5, wherein the execution unit compares the first data with the second data and compares the third data with the fourth data, and outputs new path metrics by one instruction.

7. A mobile station apparatus comprising:

the digital signal processor of claim 1.

8. A base station apparatus comprising:

the digital signal processor of claim 1.

9. A radio communication system comprising:

the digital signal processor of claim 1 mounted on at least one of a mobile station apparatus and a base station apparatus.